REMARKS

I. The Rejection

Claims 1, 2, 6 and 7 have been rejected under 35 U.S.C. § 102 (a) as anticipated by Hauge et al. (WO 01/50757 A1).

Claim 3 has been rejected under 35 U.S.C. § 103 (a) as unatentable over Hauge et al. (WO 01/50757 A1) in view of Fang (US 3,701,023).

2. Allowable Subject Matter

The Examiner indicated claims 4 and 5 would be allowable if rewritten in independent form.

3. The Amended Claims Should be Allowable

Claim 4 has been amended to independent form as requested by the Examiner to include all of the limitations of original claims 2 and 3 on which it was dependent. Claim 5 has not been changed per se since it is dependent on claim 4 and thereby incorporates all of the changes to claim 4. As amended, each of claims 4 and 5 should be allowable.

Newly added claims 8 and 9, dependent on allowable claim 4 (as herein amended), incorporate the added language of original claims 6 and 7 and should be allowable based on the allowability of claim 4.

With respect to rejected independent claims 1 and 2, language relating to "a variable frequency oscillator" included within a phase locked loop has been added to each of these claims. In addition, the recited "phase locked loop" has been further defined as having "an open loop operating condition ----- wherein an oscillator correction signal substantially equal to the average value of correction signal ----is generated, thereby causing the remodulator to operate without a correction signal, etc.". This latter added language is similar to language which is found in claim 4 and was noted by the Examiner in the "reasons for indication of allowable subject matter" as not being taught or fairly suggested by the prior art.

As such, it is respectfully submitted that independent claims 1 and 2, as amended, as well as claims 3, 6 and 7, which are dependent on claim 2,

should all be allowable as well.

A review of each of the cited references indicates that there is no mention of this open loop feature of the presently claimed arrangements, either alone or in combination with a closed loop control mode for the oscillator.

CONCLUSION

The claimed invention is not shown or suggested by Hauge et al. and neither is there any suggestion in Fang which could becombined with Hauge to arrive at the presently claimed combinations of elements. In view of the foregoing amendments to the claims and the Remarks, reconsideration and withdrawal of all of the rejections and allowance of all pending claims 1 – 9 are respectfully requested. No additional fee is required since the total number of independent claims (three) is covered by the original filing fee

Respectfully submitted,

Ronald H. Kurdyla, KPS

Attorney

Registration No. 26,932

609/734 – 6818

Patent Operations

Thomson Licensing Inc.

P.O. Box 5312, 2 Independence Way

Princeton, New Jersey 08543

September 3, 2004

CERTIFICATE OF MAILING

I hereby certify that this amendment is being deposited with the United States Postal Service as First Class Mail, postage prepaid, in an envelope addressed to the Commissioner for Patents; P.O. Box 1450; Alexandria, VA 22313-1450 on:

9/3/04
Date

Linda Tindall

Amended Claims Showing Changes

1. (Currently amended) A remodulator clock signal source, comprising:

a vestigial sideband demodulator, the demodulator being responsive to vestigial sideband transmissions containing timing information, the demodulator recovering the timing information; and

a signal path coupling the recovered timing information produced by the demodulator to a remodulator clock input so as to regulate the remodulator timing sequence, the remodulator clock signal source further comprising

a phase locked loop including a variable frequency oscillator coupled to the demodulator for generating clock pulses in response to the timing information; wherein the phase locked loop further comprises

an open loop operating condition characterized by an absence of data from the timing information wherein an oscillator correction signal substantially equal to the average value of correction signal over a recent time interval is generated, thereby causing the remodulator to operate without a correction signal from current timing information.

2. (Currently amended) A system comprising:

an input for receiving a modulated signal comprising timing information;

a demodulator coupled to the input for extracting the timing information;

a phase locked loop including a variable frequency oscillator coupled to the demodulator for generating clock pulses in response to the timing information; and

a remodulator coupled to the phase locked loop for receiving the generated clock pulses wherein

said phase locked loop has an open loop operating condition characterized by an absence of data from the timing information and wherein an oscillator correction signal substantially equal to the average value of correction signal over a recent time interval is generated, thereby causing the remodulator to operate without a correction signal from current timing information.

3, (Currently Amended) The system of claim 2, further comprising [a variable frequency oscillator, coupled to the phase locked loop,] the variable frequency oscillator receiving a correction signal from the phase locked loop based upon the source of timing information, the variable frequency oscillator thereby having an accuracy substantially equal to the source of timing information when operating in a closed loop operating condition.

4. (Currently Amended) [The] A system [of claim 3,] comprising:

an input for receiving a modulated signal comprising timing information;

a demodulator coupled to the input for extracting the timing information;

a phase locked loop coupled to the demodulator for generating clock pulses in response to the timing information;

a variable frequency oscillator, coupled to the phase locked loop, the variable frequency oscillator receiving a correction signal from the phase locked loop based upon the source of timing information, the variable frequency

oscillator thereby having an accuracy substantially equal to the source of timing information; and

a remodulator coupled to the phase locked loop for receiving the generated clock pulses;

wherein the phase locked loop further comprises:

a first closed loop operating condition characterized by the generation of the correction signal to the variable frequency oscillator based upon data from the timing information; and

a second open loop operating condition characterized by an absence of data from the timing information , thereby causing the variable frequency oscillator to operate without a correction signal.

5. (Original) The system of claim 4, further comprising:

a value register coupled to the variable frequency oscillator and maintaining a value substantially equal to the average value of the correction signal over a recent time interval; and

a multiplexer, the multiplexer selectively coupling the value from the value register to the variable frequency oscillator in the open loop operating condition, and coupling the correction signal from the phase locked loop to the variable frequency oscillator otherwise.

6. (Original) A system according to claim 2, wherein the modulated signal is a VSB modulated signal containing high definition television information.

7. (Original) A system according to claim 6, wherein the VSB modulated signal is in accordance with the ATSC standard.

8. (Newly added) A system according to claim 4 wherein the modulated signal is a VSB modulated signal containing high definition television information.

9. (Newly added) A system according to claim 8, wherein the VSB modulated signal is in accordance with the ATSC standard.